

March 1999		doc.: IEEE 802.11-990/082
N	on-linked Sou	irces
 Worst case drift timing clock sou 40 ppm 	between carrier freque rce	ency source and
1	shift for 16QAM 2,5° + 4*45°)/16 = 26.75°	
A sampling ti26.75° tolerab	hift ering of subcarriers be from -3 me shift (50 ns) corresponds t de phase shift results in a toler *32)/(26*180°) = 9.15 ns	to 26/32*180° phase shift
	n = 229 us corresponding to 5'	-
	ort and necessitates th loop for tracking of s	• • •
Submission	Slide 2	Jamshid Khun-Jush, Ericssor

	Linked Sourc	e
• Assuming a freq of sub-carrier sp	uency acquisition accu	racy in the order 2%
• With a max.	frequency error 20ppm*5GHz, or after fine frequency acquisi	· · · · ·
longer max.	frequency error whi burst length and mal ed loop for tracking of possible	kes the use of a very
	e linkage of clocks en eiver implementation	ables a reduced
Submission	Slide 3	Jamshid Khun-Jush, Ericsso